PUBLISON

DHM 89 B2

SERVICE MANUAL

CAUTION : PLEASE READ CAREFULLY CHAPTER ON

"GENERAL CONSIDERATIONS"

I GENERAL CONSIDERATIONS

1.1. Handling precautions

DHM 89 B2 contains MOS and CMOS devices, which have all protected inputs. However, it is recommended to observe usual handling precautions for electrostatic field sensitive devices : grounded soldering iron and operator. Before changing integrated circuit, connect to ground the package of the replacement device.

1.2. Special care for memories

The RAM memories of DHM have three supplies : -5 V, +5 V and +12 V. A catastrophic damage can occur if -5 V supply is suppressed, while +12 V is applied. The first measurement to make on a faulty DHM is the -5 V supply. If the -5 V is faulty, disconnect the connectors between boards E 128 and E 132, to suppress completely supplies of E 132 board (which supports RAMs), until the -5 V supply is repaired.

1.3. General test procedure

When a failure occurs, in a general way tests must be made in the following order :

- Test of the supplies
- Test of sine wave handling circuits
- Test of interface circuitry (analog to digital and digital to analog)
- Test of digital circuitry.

The diagrams C 102 and C 103 give the position of test points and components for printed boards E 128 and E 132.

For each test point, there is given, either :

- voltage (for supplies) or,
- dBm level (for sine wave) or,
- photographs of signals.

The final section gives, for each test point, the possible faulty components.

1.4. General repairing procedure

The DHM 89 B2 is mainly composed of one analog and interface board Réf. E 128, and one digital board Ref. E 132.

The E 128 board has a relatively simple schematic and is easy to repair. The E 132 board uses an original and complex wired logic, so that its functions are difficult to explain and understand, and its test requires in factory a specific test equipment.

For that reason the schematics of E 128 board are given with all details for repairing it, but a failure of E 132 board requires the replacement of it. For that purpose, we provide a standard exchange maintenance board which can be fastly exchanged with the faulty one, by simply removing four screws and two connectors. The faulty board must be returned to us for repair.

The chapter five gives the testing method by pointing out whether a failure is either on E 128 board or on E 132 board.

1.5. Caution for replacement of A/D and D/A integrated circuits

The integrated circuits of analog to digital and digital to analog converters are specially sorted out in factory for critical parameters such as offset voltage, transition time, noise, etc... If one of these circuits is broken, it is very important to replace it by a new circuit with the same order number from factory. The non-observation of this rule can create an excessive distortion.

Note : The left and right digital to analog converters being identical, the same repair kit can be used for both sides. The equivalent circuits are :

P65 = P82	P72 = P89
P66 = P83	P73 = P90
P67 = P84	P74 = P91
P68 = P85	P75 = P92
P69 = P86	P76 = P93
P70 = P87	P77 = P94
P71 = P88	P78 = P95

2 TEST OF THE SUPPLIES (E 128 BOARD)

The measurements are referenced to analog or digital ground, which are connected together in one unique point.

TP1	Digital ground
TP2	Analog ground
TP3	-15V ± 1V
TP4	+15V ± 1V
TP5	+5V ± 0,25V (Digital supply)
TP5B	+5V ± 0,25V (Analog reference supply)
TP6	+12V ± 1V
TP7	-8V ± 0,2V
TP8	+7,5V ± 0,5V
TP9	-5V ± 0,5V

3 TEST OF SINE WAVE HANDLING CIRCUITS

The following test points must all give sine wave, when sine wave is applied to inputs of DHM.

The test conditions are :

Feedback :	0
Mode :	Delay
	True Stereo
Bandwidth :	10 kHz
Input gain :	0 dB (position of potentiometer)
Input level:	0 dBm
Input frequency :	1000 Hz

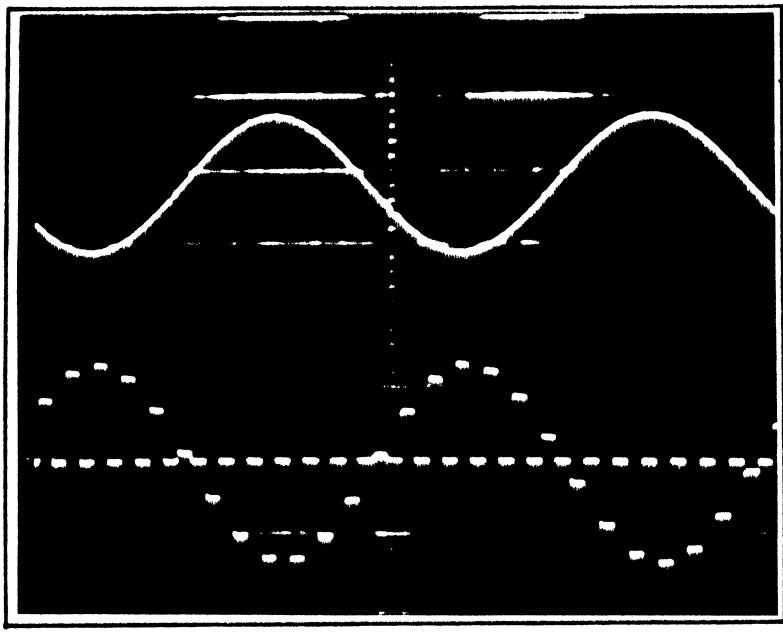
The other settings of DHM have no influence on measurement.

The following levels must be found :

TP 14 - TP 17 - TP 22 - TP 23 - TP 42 - TP 56	- 6 dBm
TP 18 - TP 13 - TP 20 - TP 21 - TP 24 - TP 25	- 9 dBm
TP 15 - TP 16	0 dBm

4 TEST OF INTERFACE CIRCUITS

The following photographs give signals for analog to digital and digital to analog converters. For these tests, the feedbacks are on "0", the left input gain on "0 dB " and the right input gain on " - ∞"

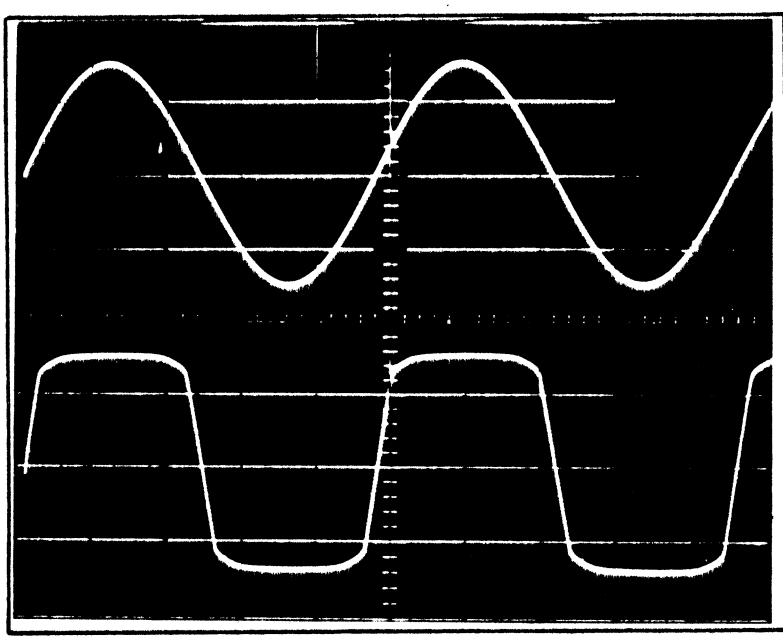


TEST POINT N° 25 Top
26 Bottom

TEST CONDITIONS :
MODE : { True Stereo
Delay

BANDWIDTH : 10 kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : On
INPUT LEVEL : + 5 dBm
INPUT FREQUENCY : 2000 Hz

SCOPE VERTICAL : 1 V /DIV
HORIZONTAL 0,1 mS /DIV

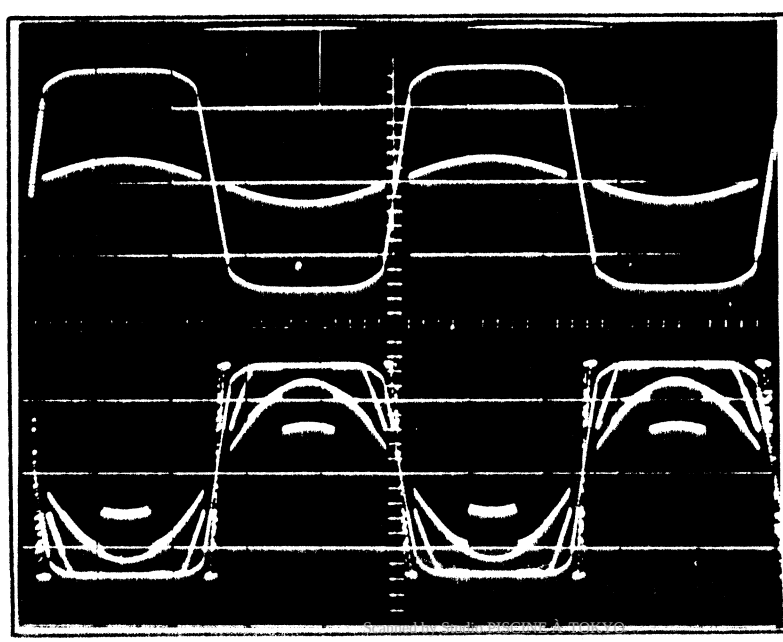


TEST POINT N° 26 Top
26B Bottom

TEST CONDITIONS :
MODE : { Quasi Stereo
Delay

BANDWIDTH : 20 kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : On
INPUT LEVEL : + 15 dBm
INPUT FREQUENCY : 100 Hz

SCOPE VERTICAL : 1 V Top /DIV
5 V Bot
HORIZONTAL : 2 mS /DIV

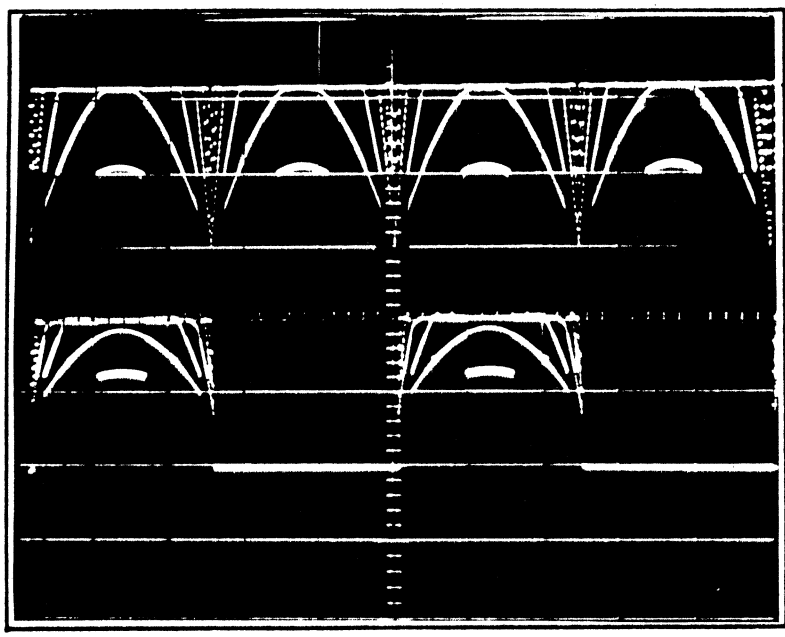


TEST POINT N° 26 C Top
26 D Bottom

TEST CONDITIONS :
MODE : { Quasi stereo
Delay

BANDWIDTH : 20 kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : On
INPUT LEVEL : + 15 dBm
INPUT FREQUENCY : 100 Hz

SCOPE VERTICAL : 5 V /DIV
HORIZONTAL : 2 mS /DIV



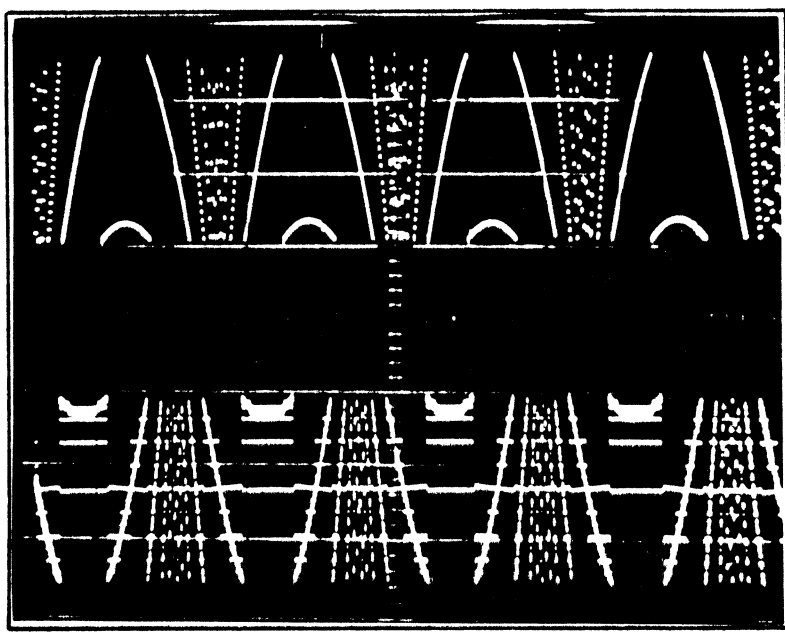
TEST POINT N° 26 E Top
26 F Bottom

TEST CONDITIONS :

MODE : { Quasi stereo
Delay

BANDWIDTH : 20 kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : On
INPUT LEVEL : + 15 dBm
INPUT FREQUENCY : 100 Hz

SCOPE VERTICAL : 5 V /DIV
HORIZONTAL : 2 mS /DIV



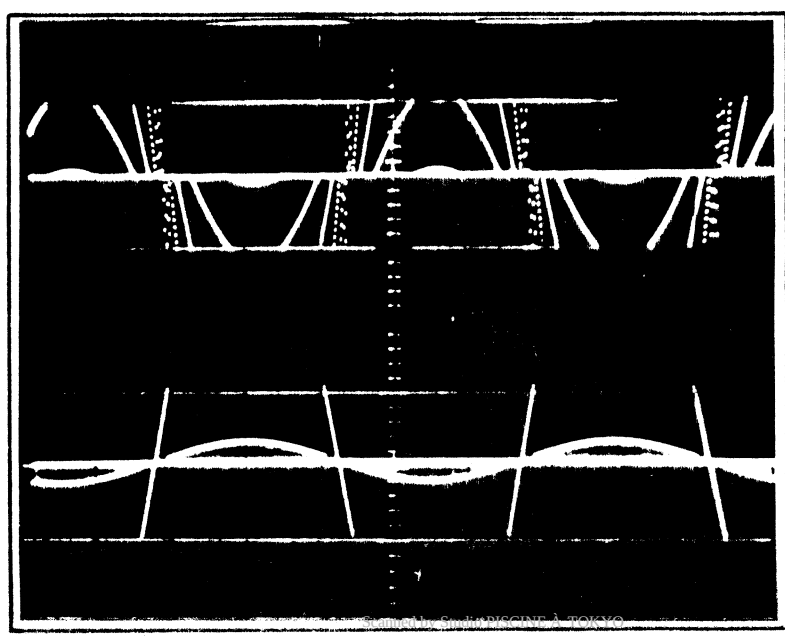
TEST POINT N° 27 Top
28 Bottom

TEST CONDITIONS :

MODE : { Quasi stereo
Delay

BANDWIDTH : 20 kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : On
INPUT LEVEL : + 15 dBm
INPUT FREQUENCY : 100 Hz

SCOPE VERTICAL : 5 V /DIV
HORIZONTAL : 2 mS /DIV



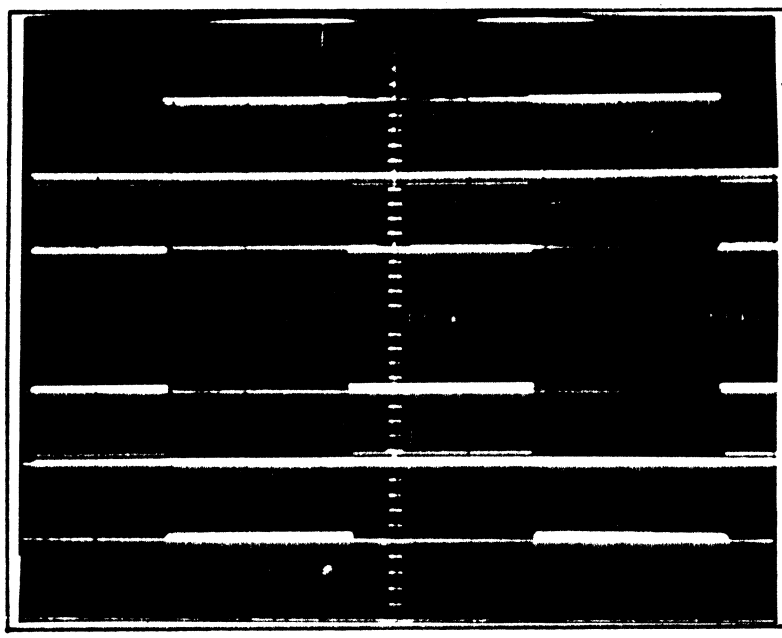
TEST POINT N° 41-55 Top
41B-55B Bot.

TEST CONDITIONS :

MODE : { Quasi-stereo
Delay

BANDWIDTH : 20 kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : On
INPUT LEVEL : + 15 dBm
INPUT FREQUENCY : 100 Hz

SCOPE VERTICAL : 5 V /DIV
HORIZONTAL : 2 mS /DIV



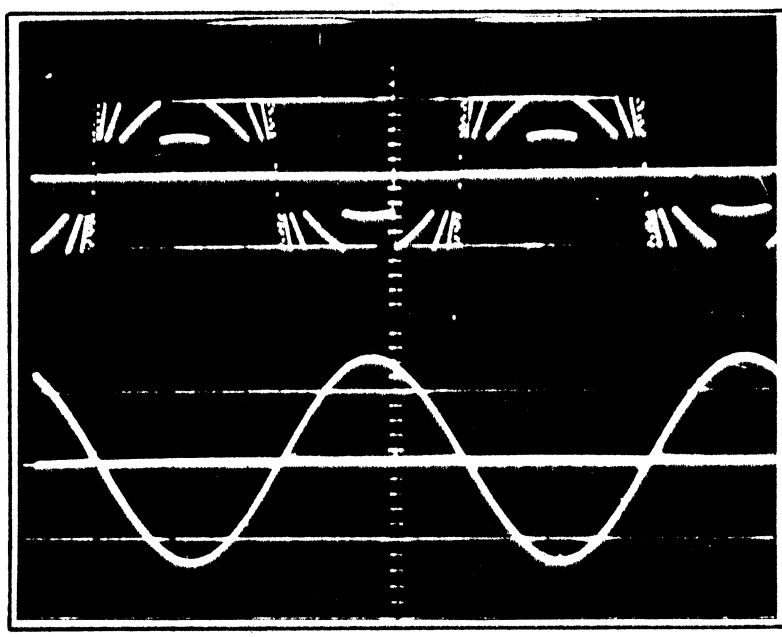
TEST POINT N° 41C-55C Top
41D-55D Bot.

TEST CONDITIONS :

MODE : { True stereo
Delay

BANDWIDTH : 20 kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : On
INPUT LEVEL : + 15 dBm
INPUT FREQUENCY : 100 Hz

SCOPE VERTICAL : 5 V /DIV
HORIZONTAL : 2 mS /DIV



TEST POINT N° 41E-55E Top
41F-55F Bot.

TEST CONDITIONS :

MODE : { True stereo
Delay

BANDWIDTH : 20 kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : On
INPUT LEVEL : + 15 dBm
INPUT FREQUENCY : 100 Hz

SCOPE VERTICAL : 5 V Top /DIV
1 V Bot /DIV
HORIZONTAL : 2 mS /DIV

TEST POINT N°

TEST CONDITIONS :

MODE : {

BANDWIDTH :
DELAY :
CROSSPOINT 1 :
CROSSPOINT 2 :
RATIO :
ENVELOPE SYNCHRO :
INPUT LEVEL :
INPUT FREQUENCY :

SCOPE VERTICAL : /DIV
HORIZONTAL : /DIV

5 LOCALISATION OF A FAILURE

(Note : In the following discussion, it is supposed that power supplies are correct).

5.1. Test of inputs of A/D convertor (TP 24 and TP 25)

- Refer to chapter 3 for testing TP 24 and TP 25.
- If TP 24 (for right channel) or TP 25 (for left channel) are defective, the fault is either on board E 128, or on front panel boards E 130 (which support input gain amplifiers).

  (Note : In quasi-stereo mode, the two inputs are mixed together on TP 25).

5.2. Test of Analog to Digital converter

- Test the five clocks of AD converter : TP 109, TP 110, TP 111, TP 112; TP 130.
  If they are defective, the fault is on the digital board E 132.
- Test the internal signals TP 26 to TP 28, inside the A/D Converter. If they are defective and if TP 109 to TP 112 are correct, the fault is inside A/D converter itself. Try to change integrated circuits P 34 to P 55. If the fault still appears, check the following discrete components : R 113 to R 175 - C 57 to C 79 - D 16 to D 39.
- Test the input of memories, TP 87 to TP 98.
- If the previous tests are correct, and if TP 87 to TP 98 are defective, try to change the following latches and buffers of A/D converter output : P 56, P 57, P 58, P 59.

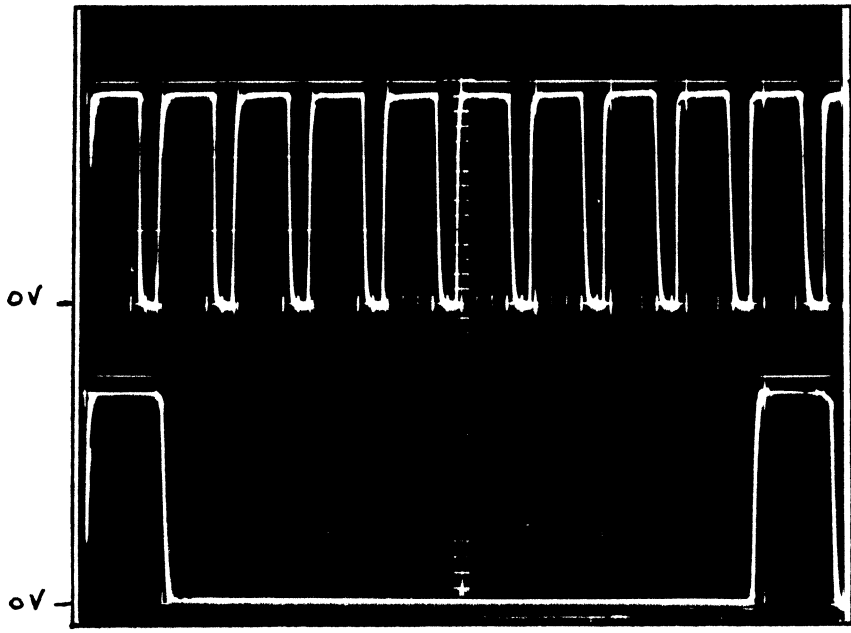
Note 1 : If the circuits P 37 or P 40 are changed, it is necessary to adjust trimmers PM2 and PM3 :

- Put the DHM in delay and quasi-stereo mode
- Set the "input gain" potentiometers on 0dB, and the bandwidth on 10 kHz.
- Enter a signal 1000 Hz, - 10 dBm on one input only (left or right).
- Connect an harmonic distorsion meter on one output of DHM.
- Adjust PM3 for the minimum distorsion (THD typically between 0,12 and 0,15 %).
- Then enter a signal 1000 Hz, 0dBm
- Adjust PM2 for the minimum distorsion (THD typically between 0,08 and 0,1 %)

Note 2 : PM1 and PM4 are used only for factory tests. The normal settlings are :

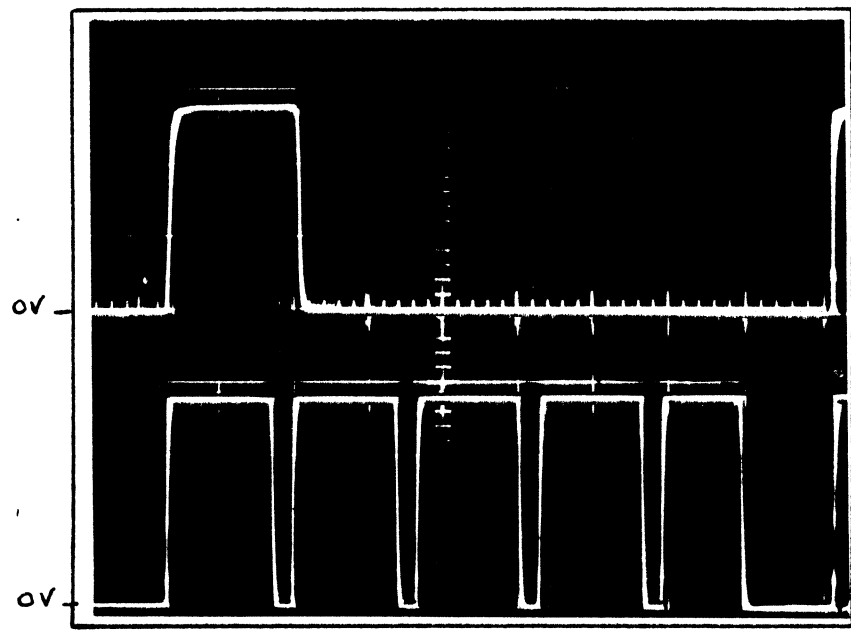
- Completely counterclockwise for PM1
- Mid-position for PM4.

Note 3 : The DHM uses a 16 bit flying comma A/D converter. The digital dynamic is the same as for a 16 bit linear converter, but the code is condensed onto a twelve bit format. The advantage is a longer delay for the same memory capacity.



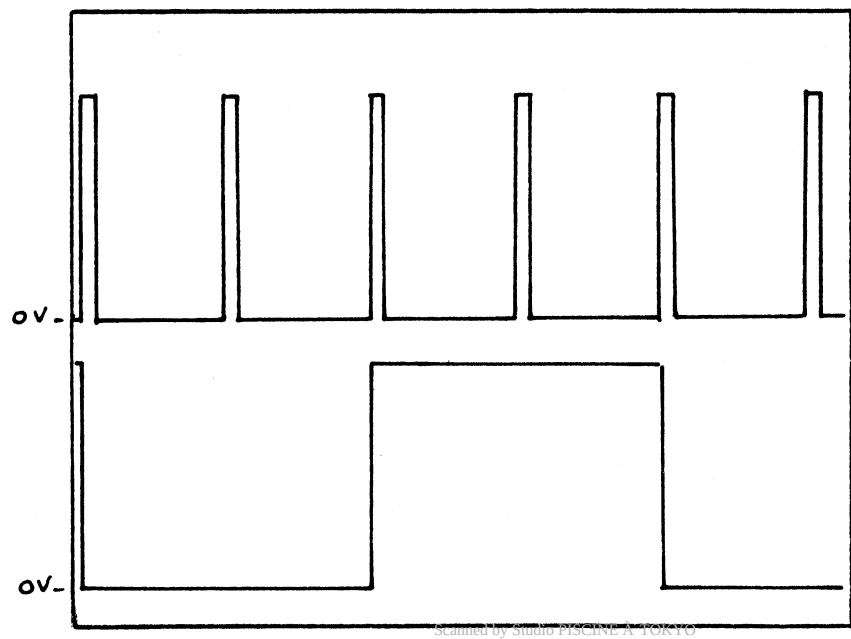
TEST POINT N° 109 Top.
110 Bottom.

TEST CONDITIONS :
MODE : { Don't care
BANDWIDTH : "
DELAY : "
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : "
INPUT LEVEL : "
INPUT FREQUENCY : "
SCOPE SYNCHRO : TP110
SCOPE VERTICAL : 5 V /DIV
HORIZONTAL : 2 µS /DIV



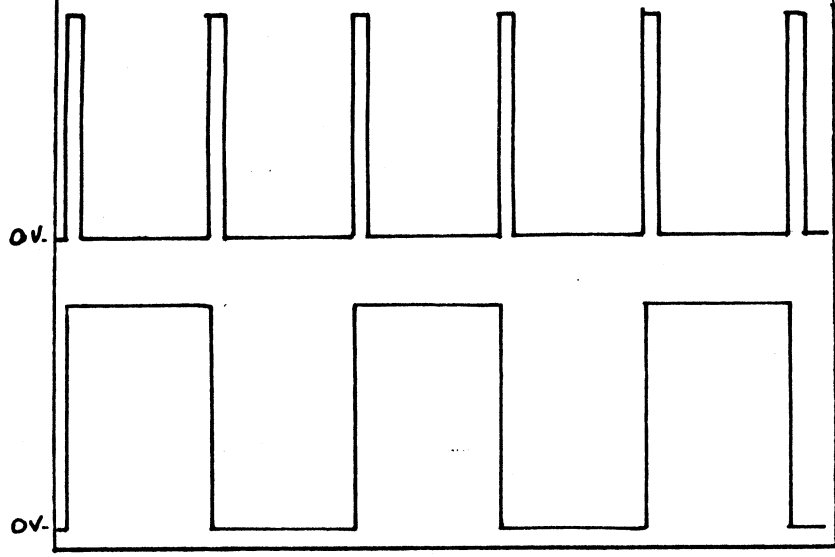
TEST POINT N° 111 Top
112 Bottom

TEST CONDITIONS :
MODE : { Don't care
BANDWIDTH : "
DELAY : "
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : "
INPUT LEVEL : "
INPUT FREQUENCY : "
SCOPE SYNCHRO : TP 110
SCOPE VERTICAL : 5V /DIV
HORIZONTAL : 2 µS /DIV



TEST POINT N° 110 Top
130 Bottom

TEST CONDITIONS :
MODE : { Don't care
BANDWIDTH : 5 kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : "
INPUT LEVEL : "
INPUT FREQUENCY : "
SCOPE VERTICAL : 5V /DIV
HORIZONTAL : 10 µS /DIV

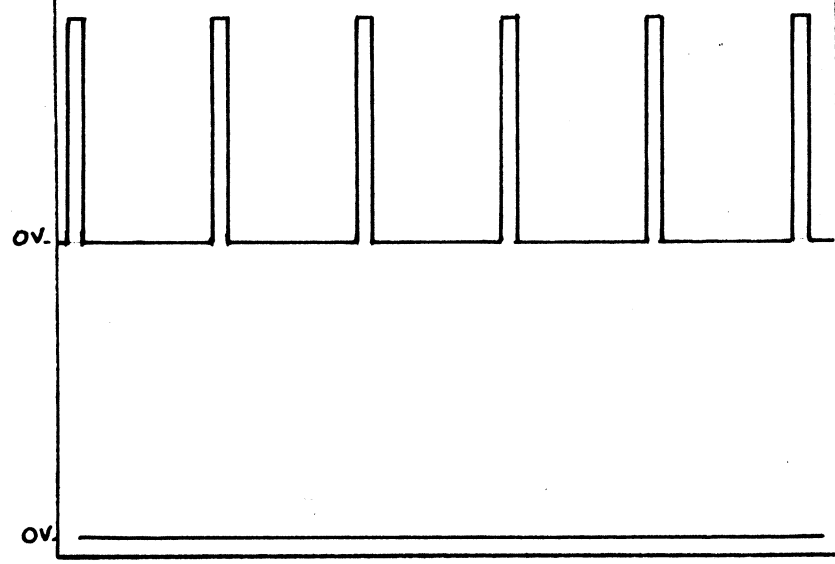


TEST POINT N° 110 Top
130 Bottom

TEST CONDITIONS :
MODE : { Don't care

BANDWIDTH : 10 kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : "
INPUT LEVEL : "
INPUT FREQUENCY : "

SCOPE VERTICAL : 5V /DIV
HORIZONTAL : 10 S /DIV



TEST POINT N° 110 Top
130 Bottom

TEST CONDITIONS :
MODE : { Quasi-stéréo

BANDWIDTH : 20 kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : "
INPUT LEVEL : "
INPUT FREQUENCY : "

SCOPE VERTICAL : 5V /DIV
HORIZONTAL : 10 S /DIV

Memory imputs :

Square waves with random phase and frequency, depending upon the frequency and the level of imput signals.

They are the multiplexed result of A/D conversions.

Low level : 0 V
High level: 3,5 V for TP 87 to TP 90
5 V for TP 91 to TP 98

TEST POINT N° 87 to 98

TEST CONDITIONS :
MODE : { Don't care

BANDWIDTH : "
DELAY : "
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : "
INPUT LEVEL : "
INPUT FREQUENCY : "

SCOPE VERTICAL : /DIV
HORIZONTAL : /DIV

5.3. Test of the digital board E 132 outputs

- Test the logic control signals of D/A conversion :
  TP 205, TP 206 and TP 221 for left channel
  TP 305, TP 306 and TP 321 for right channel
- If one of these is wrong, the E 132 board is defective. Replace it.
- Test the latched memories outputs :
  TP 43 to TP 54 for left channel, TP 29 to TP 40 for right channel. If they are defective, when the input A/D converter is correct, the following possibilities are :
  - Defective memory buffers : P 60, P 61 and P 62 with pull-up resistors R 176 to R 187.
  - Defective latches : P 80 - P 81 for left channel
    P 63 - P 64 for right channel
  - Defective E 132 board. Then, replace it.

5.4. Test of digital to analog converters

- Refer to chapter 4 for testing the D/A converters
  TP 55 to TP 55 F - TP 561 - TP 562 - TP 56 for left channel
  TP 41 to TP 41 F - TP 421 - TP 422 - TP 42 for right channel
  If they are defective when latched memory outputs and control signals are correct, the following components can be defective :
  P 82 to P 96 - R 218 to R 244 - C 90 to C 100 - D 44 to D 47 for left channel
  P 65 to P 79 - R 188 to R 217 - C 80 to C 89 - D 40 to D 43 for right channel

Note 1 : Each channel uses two decoded outputs, which are then mixed to obtain each output.
Left channel uses outputs TP 561 and TP 562 which are mixed on TP 56.
Right channel uses TP 421 and TP 422 which are mixed on TP 42.
In delay mode, one of the two basic outputs is used only while the other is null. If a change in delay settling occurs, the previous active output becomes null while the previous null output becomes active .

Note 2 : If integrated circuits P 88 to P 92 are replaced for left channel, it is necessary to adjust the PM 7 trimmer (respectively P 71 to P 75 and PM5 for right channel) :

- Put the DHM in mode delay, quasi stereo, 10 kHz bandwidth
- Preset input gains on "0dB"
- Apply on one input only a 1000 Hz, 0dBm sine wave
- For left channel, connect an AC millivoltmeter to the output, TP 561 or TP 562, which is null. The ground of millivoltmeter must be connected to analog ground of DHM. It is recommended to use a high frequency rejection filter, to suppress high frequency noise. A simple R-C low-pass network, with R = 100 Ω and C = 0,1 µF is sufficient. The result is a better

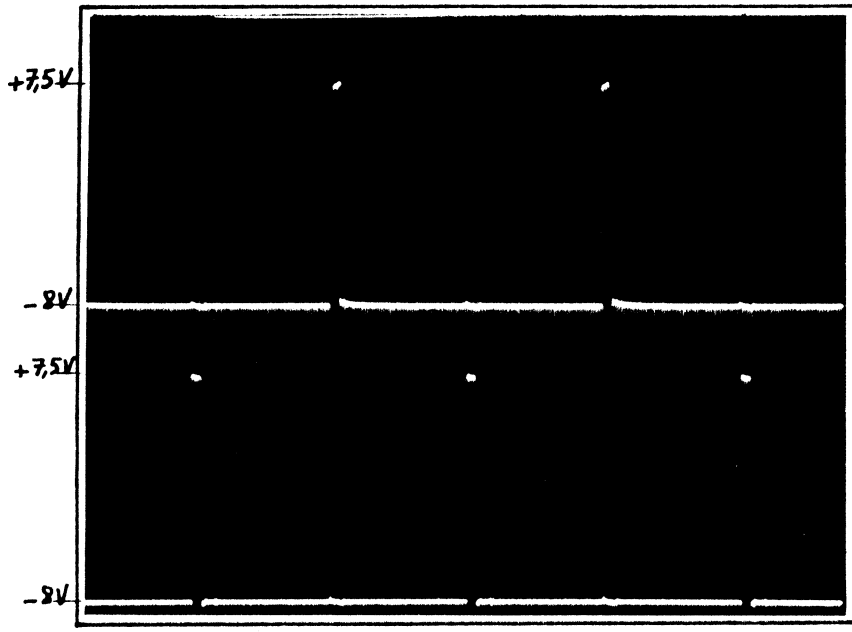
sensitivity for settling PM 7. PM 7 must be settled with a view to obtain the lowest possible reading on AC millivoltmeter, typically less than 1 m V.
- For right channel, operation is similar but with TP 421 or TP 422 and PM 5 trimmer.

Note 3 : PM 8 (for left channel) and PM 6 (for right channel) adjust the balance of the two basic decoded outputs mixing of each channel. The replacement of integrated circuits has no influence on these settlings.
However, if there is an accidental shift, the settling procedure is as follows :

- Put the DHM in pitch-shifting, quasi-stereo mode, 10 kHz bandwidth.
- Adjust pitch-ratio = 1,20; crosspoint 1 = 100 mS crosspoint 2 = 400 mS; input gain = 0dB
- Enter a 200 Hz 0dBm sine-wave.
- Connect an AC millivoltmeter on the tested DHM output.
- If the balance is wrong, a periodical change in level occurs. Adjust PM8 (for left channel) and PM 6 (for right channel) to null this variation and get a well regular sine-wave output.

5.5. Test of output analog circuitry

- Refer to chapter 3 for sine-wave output measurements.
- If D/A decoder outputs are correct and general output of DHM wrong, test successively the output filters, the keyboard insertion switching and the output amplifiers.



TEST POINT N° 205 (305) Top.
206 (306) Bot.

TEST CONDITIONS :
MODE : { Delay

BANDWIDTH : 10kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : "
INPUT LEVEL : "
INPUT FREQUENCY : "

SCOPE VERTICAL : 5 V /DIV
HORIZONTAL : 10µS /DIV

Notes for test points TP 205 - 206 - 305 -306:

- The positive pulses duration is : 1,0µS.
- The interval between pulses is function to bandwidth selection and pitch-ratio its typical value is :

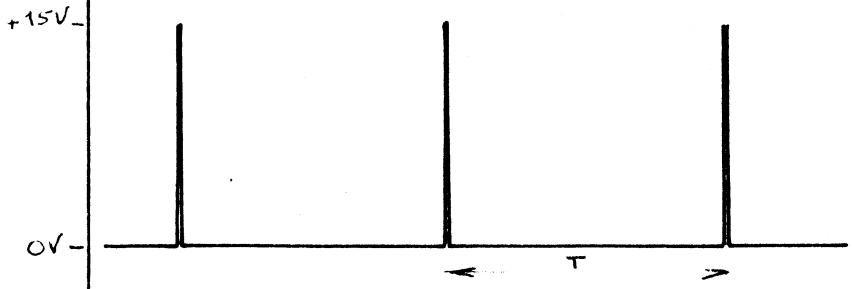
T = 18,9 µS for Pitch-ratio = 1,00 ; 20kHz
T = 9,45µS for Pitch-ratio = 2,00 ; 20kHz
T = 37,8 µS for Pitch-ratio = 1,00 ; 5kHz
T = 75,6 µS for Pitch-ratio = 1,00 ; 5kHz

TEST POINT N°

TEST CONDITIONS :
MODE : {

BANDWIDTH :
DELAY :
CROSSPOINT 1 :
CROSSPOINT 2 :
RATIO :
ENVELOPE SYNCHRO :
INPUT LEVEL :
INPUT FREQUENCY :

SCOPE VERTICAL : /DIV
HORIZONTAL : /DIV



Note :

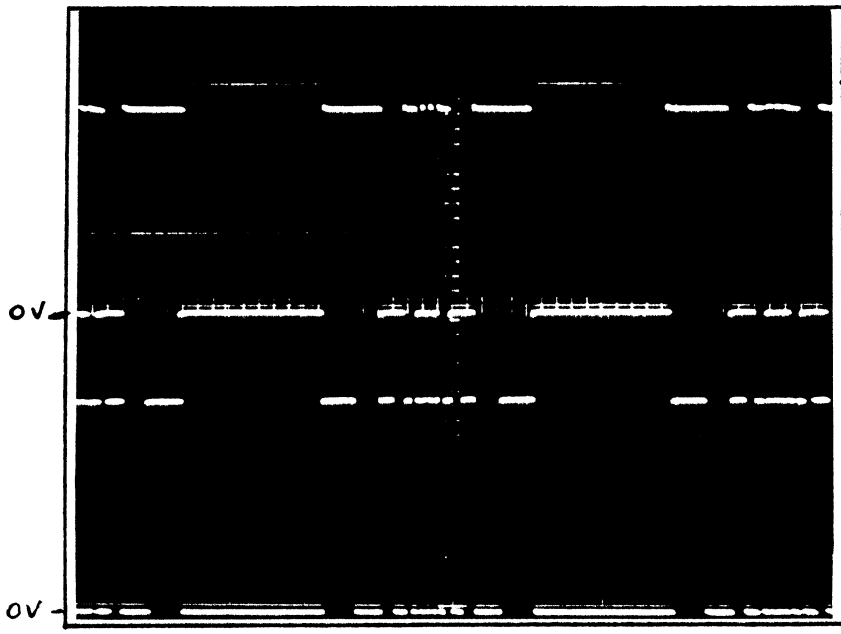
- Positive pulse duration 50 nS.
- Interval between pulses is variable but is a multiple of 0,7µS.
  Typical value :
  T = 18,9µS for delay mode, 20kHz.

TEST POINT N° 221 - 321

TEST CONDITIONS :
MODE : {

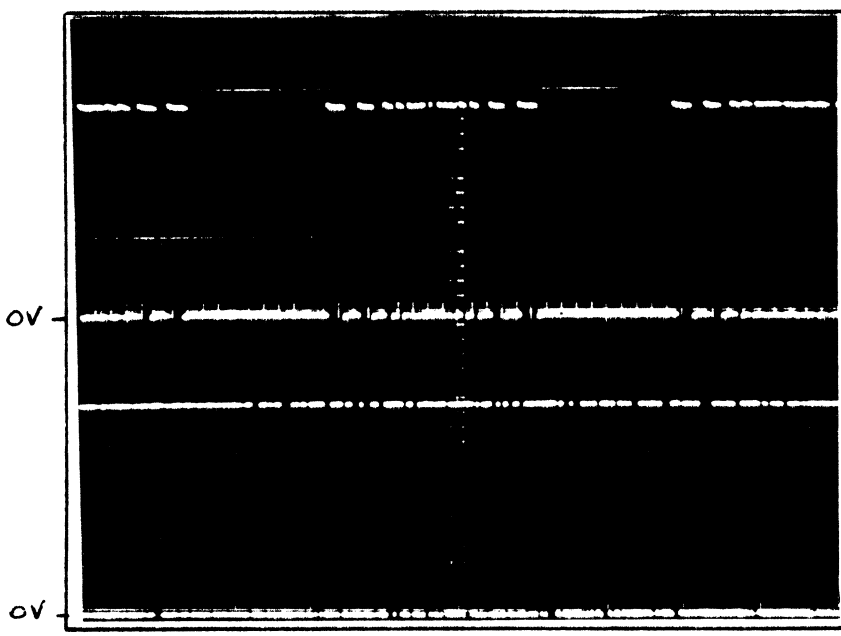
BANDWIDTH :
DELAY :
CROSSPOINT 1 :
CROSSPOINT 2 :
RATIO :
ENVELOPE SYNCHRO :
INPUT LEVEL :
INPUT FREQUENCY :

SCOPE VERTICAL : 5 V /DIV
HORIZONTAL : /DIV



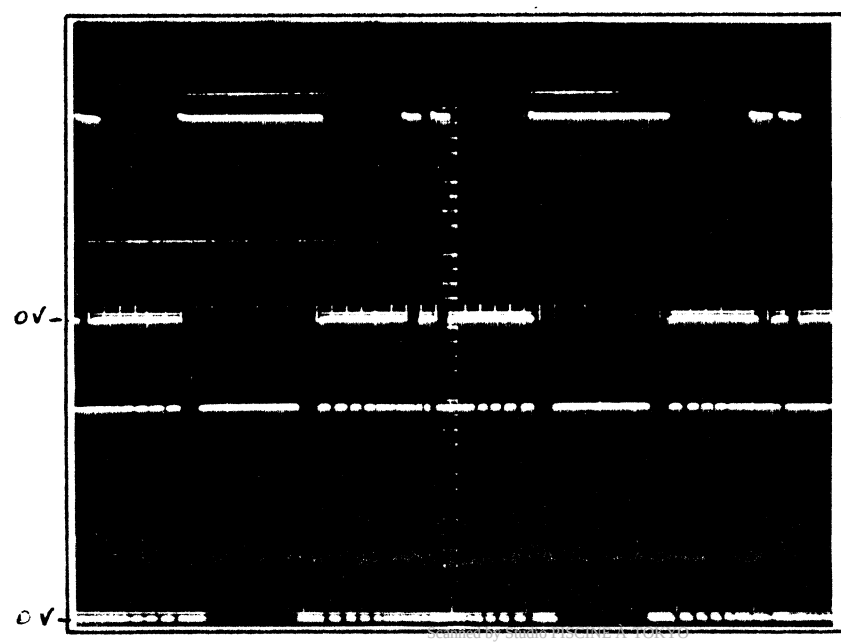
TEST POINT N° 29 - 43 Top
30 - 44 Bot.

TEST CONDITIONS :
MODE : { Delay
Quasi-stereo
BANDWIDTH : 20 kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : "
INPUT LEVEL : + 15 dBm
INPUT FREQUENCY : 100 Hz
INPUT GAIN : OdB
SCOPE VERTICAL : 5 V /DIV
HORIZONTAL : 1mS /DIV



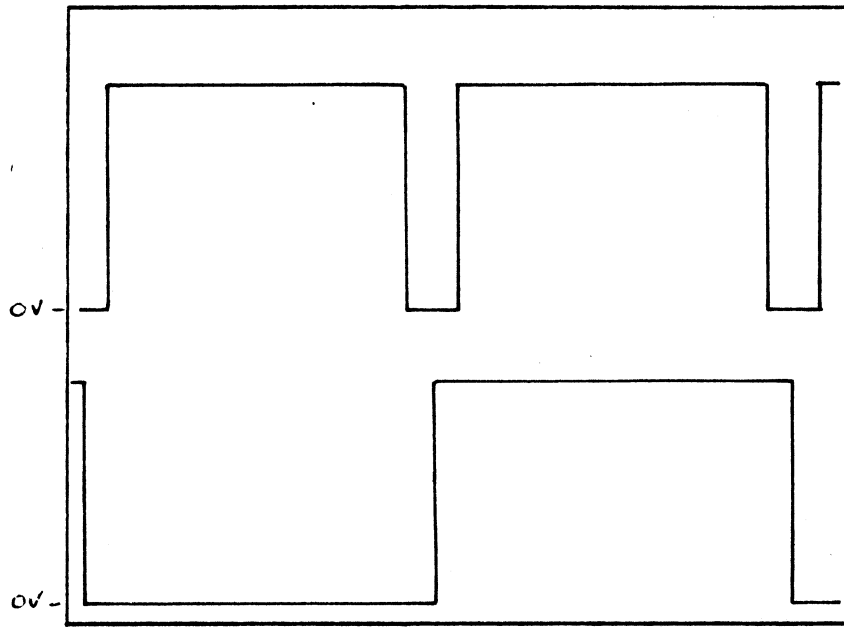
TEST POINT N° 1 - 45 Top
35 - 49 Bot.

TEST CONDITIONS :
MODE : { Delay
Quasi-stereo
BANDWIDTH : 20 kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : "
INPUT LEVEL : + 15 dBm
INPUT FREQUENCY : 100 Hz
INPUT GAIN : OdB
SCOPE VERTICAL : 5 V /DIV
HORIZONTAL : 1mS /DIV



TEST POINT N° 32 - 46 Top
40 - 54 Bot.

TEST CONDITIONS :
MODE : { Delay
Quasy-stereo
BANDWIDTH : 20 kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : "
INPUT LEVEL : + 15 dBm
INPUT FREQUENCY : 100 Hz
INPUT GAIN : OdB
SCOPE VERTICAL : 5 V /DIV
HORIZONTAL : 1mS /DIV

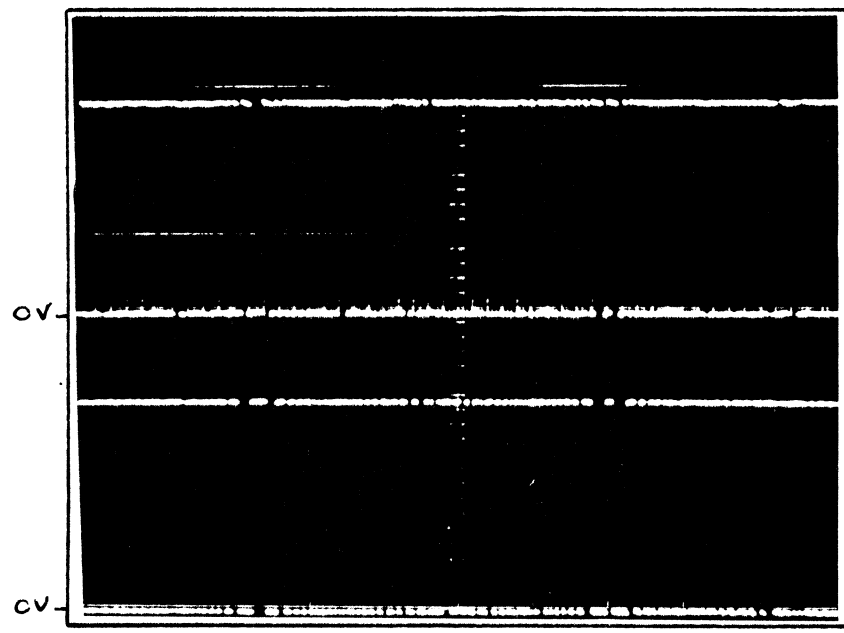


TEST POINT N° 34-48 Top / 33-47 Bot.

TEST CONDITIONS :

MODE : { Delay / Quasi-stereo

BANDWIDTH : 20kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : "
INPUT LEVEL : + 15dBm
INPUT FREQUENCY : 100Hz
INPUT GAIN : OdB
SCOPE VERTICAL : 5 V /DIV
HORIZONTAL : 1mS /DIV

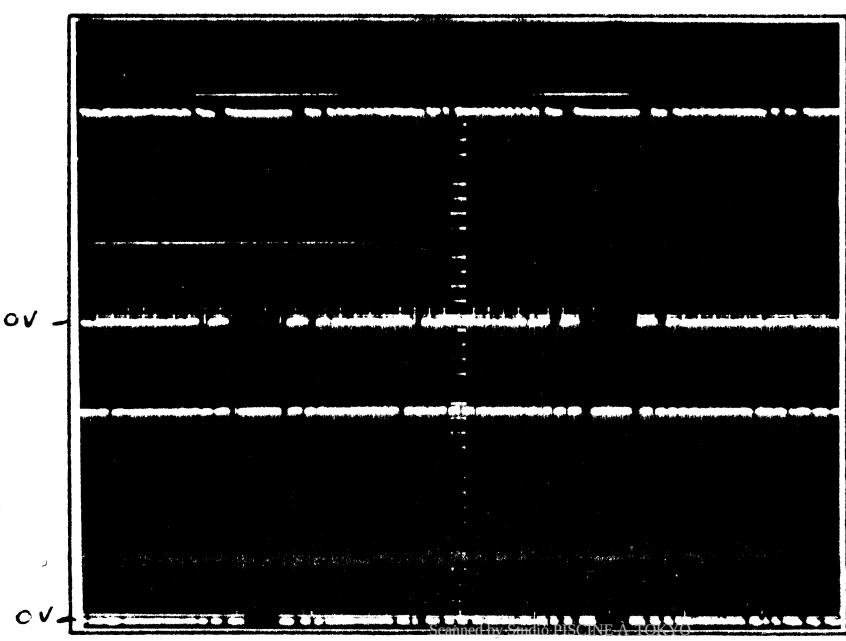


TEST POINT N° 36 - 50 Top / 37 - 51 Bot.

TEST CONDITIONS :

MODE : { Delay / Quasi-stereo

BANDWIDTH : 20kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : "
INPUT LEVEL : + 15dBm
INPUT FREQUENCY : 100Hz
INPUT GAIN : OdB
SCOPE VERTICAL : 5 V /DIV
HORIZONTAL : 1mS /DIV



TEST POINT N° 39 - 53 Top / 38 - 52 Bot.

TEST CONDITIONS :

MODE : { Delay / Quasi-stereo

BANDWIDTH : 20kHz
DELAY : Don't care
CROSSPOINT 1 : "
CROSSPOINT 2 : "
RATIO : "
ENVELOPE SYNCHRO : "
INPUT LEVEL : + 15dBm
INPUT FREQUENCY : 100 Hz
INPUT GAIN : OdB
SCOPE VERTICAL : 5 V /DIV
HORIZONTAL : 1mS /DIV

COMPONENTS LIST - INTEGRATED CIRCUITS

Diagram N°	Reference	Manu-facturer
P1	TL 071 CP	T.I.
P2	"	"
P3	"	"
P4	"	"
P5	"	"
P6	"	"
P7	"	"
P8	"	"
P9	"	"
P10	"	"
P11	CD 4066 BE	RCA
P12	TL 071 CP	T.I.
P13	"	"
P14	CD 4066 BE	RCA
P15	"	"
P16	"	"
P17	"	"
P18	"	"
P19	TL 071 CP	T.I.
P20	"	"
P21	"	"
P22	"	"
P23	CD 4066 BE	RCA
P24	"	"
P25	"	"
P26	"	"
P27	"	"
P28	TL 071 CP	T.I.
P29	"	"
P30	CD 4066 BE	RCA
P31		
P32	TL 071 CP	T.I.
P33	"	"
P60	SN 74LS26 N	T.I.
P61	"	"
P62	"	"
P63	CD 40174 BE	RCA
P64	"	"
P79	TL 071 CP	T.I.
P80	CD 40174 BE	RCA
P81	"	"
P96	TL 071 CP	T.I.

Diagram N°	Reference	Manu-facturer
P97	TL 064 CN	T.I.
P98	TL 071 CP	"
P99	"	"
P100	RC 4151 NB	Raytheon
P101	NE 566 V	RTC
P102	SN 74LS02 N	T.I.
P103	CD 4066 BE	RCA
P104	TL 084 CN	T.I.
P105	CD 4066 BE	RCE
P106	SN 74LS74 N	T.I.
P107	CE 4066 BE	RCA
P108	"	"
P109	TL 064 CN	T.I.
P110	SN 74LS26 N	T.I.
P111	SN 74LS74 N	"
P112	TL 071 CP	"
P113	RC 4151 NB	Raytheon
P114	NE 566 V	RTC
P115	SN 74LS02 N	T.I.
P116	CD 4066 BE	RCA
P117	"	"
P118	"	"
P119	TL 084 CN	T.I.
P120	SN 74LS26 N	"
P121	TL 064 CN	"
P122	SN 74LS08 N	"
P123	TL 062 CP	"

Note : T.I. = Texas Instruments